International Journal of Research in Engineering, Science and Management
Volume-3, Issue-1, January-2020
www.ijresm.com | ISSN (Online): 2581-5792

Design of 4x2 Priority Encoder Using Reversible Logic Gates

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***Abstract*: Reversible logic gate has gained importance in recent times due to its low power dissipation and it is important in low power design. On the other hand, it has low power consumption and it has applications in reversible logic. In this project, a 4x2 priority encoder is proposed which is based on reversible logic. Basically Reversible Logic Gates contains n×n mapping so that we can easily retrieve our output from input. But in case of normal conventional gates it not possible. Firstly, this project discusses about design of Fredkin gate and Universal Reversible Logic Gate (URLG). Secondly, this project uses reversible logic gate (both Fredkin and URLG) to design a 4x2 priority encoder. As minimizes the garbage count and also reduction in size hence it is chosen for designing 4x2 priority encoder.**

***Keywords*: Reversible logic gate, Fredkin gate, Universal reversible logic gate (URLG), Priority encoder.**

1. Introduction

An encoder circuit, outputs an encoded value based on the states of all the inputs to the encoder circuit [1]. A priority encoder can be established as a circuit that compresses multiple several binary inputs into a smaller range of outputs and produces an output that's the binary illustration of the authentic wide variety starting from zero of the maximum important input bit. By acting on the highest priority encoder they are often used to control interrupt requests. If two or more inputs are given at the same time to the encoder, the input having the highest priority takes the lead. Different types of priority encoders include 4 to 2, 8 to 3 priority encoders [2].

A reversible logic gate is defined as a circuit with equal number of inputs and outputs and one to one mapping from input to output [3]. Reversible logic is an emerging technology with promising applications because of the low power dissipation [4]. The power dissipation of reversible logic circuits under ideal circumstance is zero. There is no unavoidable energy consumption in reversible logic computers [5]. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs [6].Reversibility in computing implies that no information A reversible logic gate is defined as a circuit with equal number of inputs and outputs and one to one mapping from input to output [7].Reversible logic is an emerging technology with promising applications because of the low power dissipation [8]. The power dissipation of reversible logic circuits under ideal circumstance is zero. There is no unavoidable energy consumption in reversible logic computers [9]. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs [10]. Reversibility in computing implies that no information about the computational states can ever be lost, so we will recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility are often gained only after employing physical reversibility [11]. Physical reversibility may be a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to at least one. Most of the energy needed to form that change is given off within the sort of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to subsequent. This way, one can only expect to lose a moment amount of energy on each transition. Reversible computing strongly affects digital logic designs [12]. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages also. Eventually, these also will need to be reversible to supply optimal efficiency. High-performance chips releasing large amounts of warmth impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by uncomputing bits rather than throwing them away, will soon offer the sole physically possible thanks to keep improving performance. A reversible gate is an n-input n-output logic device with one-to-one mapping [13]. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also within the synthesis of reversible circuits direct fan-Out isn't allowed as one–to-many concepts isn't reversible. However, fan-out in reversible circuits is obtained using extra gates. A reversible circuit should be composed using minimum number of reversible logic gates [14]. From the purpose of view of reversible circuit design,

there are numerous parameters for determining the complexity and performance of circuits.

1. The number of Reversible gates (N): The number of reversible gates here in this circuit.
2. The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at
3. Either 0 or 1 in order to synthesize the given logical function.
4. The number of garbage outputs (GO): which refers to the number of unused outputs present in a reversible logic circuit. these are inevitable and the rubbish outputs as these are very much required to realize reversibility.
5. Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the amount of primitive reversible logic gates (1*1 or 2*2) required to understand the circuit.

The important reversible gates we have here for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate, recently developed Gate sayem gate and peres gate etc. [15].

2. Existed Priority encoder model

Generally, digital encoders produce outputs of 2-bit, 3-bit or 4-bit codes depending upon the number of data input lines. An “n-bit” binary encoder has 2n input lines and n-bit output lines with common types that include 4-to-2, 8-to-3 and 16-t line configuration.

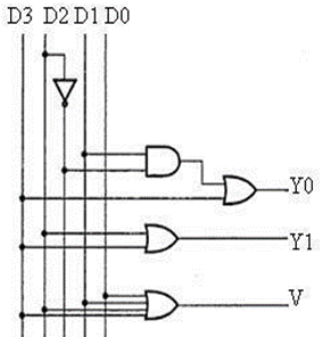

Fig. 1. Existed block diagram of priority encoder

3. Proposed method

In this section, design of a reversible logic based 4x2 priority encoder is proposed using Fredkin gate and URLG. In priority encoder if two or more inputs are high at the same time, then the input with highest priority takes precedence. The logic truth table of 4x2 priority encoder is shown in table 4, where I0, I1, I2and I3 are four line inputs, Y1 and Y0 are the final encoded output according to the priority of the input signal taking precedence. From Table 4, it is also seen that the priority order is from high to low, i.e. I3, I2, I1 and I0. Therefore, for example if I3 and I2 both are high at a time then only I3 is encoded. From the truth table, the logic expression for the priority encoder can be written as,

Y1=I2+I3

Y2=I3+I2'I1

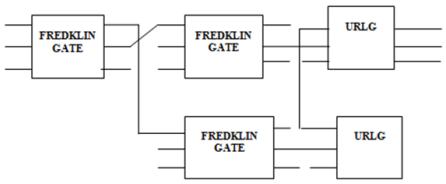

Fig. 2. Proposed block diagram of priority Encoder Using Reversible logic gates

A. *Fredkin Gate*

The Fredkin gate (also CSWAP gate) is a computational circuit suitable for reversible computing, invented by Fredkin. It is universal, which suggests that any logical or mathematical process are often constructed entirely of Fredkin gates. The Fredkin gate may be a circuit or device with three inputs and three outputs that transmits the primary bit unchanged and swaps the last two bits if, and only if, the first bit is 1[16]. The basic Fredkin gate may be a controlled swap gate that maps three inputs (C, I1, I2) onto three outputs (C, O1, O2).

The C input is mapped on to the C output. If C = 0, no swap is performed; I1 maps to O1, and I2 maps to O2. Otherwise, the 2 outputs are swapped in order that I1 maps to O2, and I2 maps to O1. It is easy to ascertain that this circuit is reversible, i.e., "undoes" itself when run backwards. A generalized n×n Fredkin gate passes its first n-2 inputs unchanged to the corresponding outputs, and swaps its last two outputs if and as long as the primary n-2 inputs are all 1. It has the useful property that the numbers of 0s and 1s are conserved throughout, which within the ball model means an equivalent number of balls are output as input.

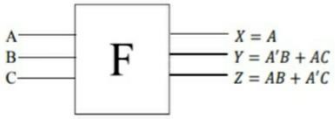

Fig. 3. Fredkin gate

The Fredkin gate can be defined using truth functions with AND, OR, XOR, and NOT, as follows:

O1 = I1 XOR S

O2 = I2 XOR S

Cout= Cin

Where S = (I1 XOR I2) AND C

Alternatively:

O1 = (NOT C AND I1) OR (C AND I2)

O2 = (C AND I1) OR (NOT C AND I2)

Table 1
Truth table of Fredkin gate

Inputs			Outputs		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

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4. Results

A. RTL schematic of Fredkin Gate

Here we designed the Fredkin Gate which is the one of the popular conservative reversible logic gate where A, B, C are inputs and X, Y, Z are outputs respectively. The Fredkin Gate itself Consists of number of And gates, or gates we can reduce the gate count in complex circuits.

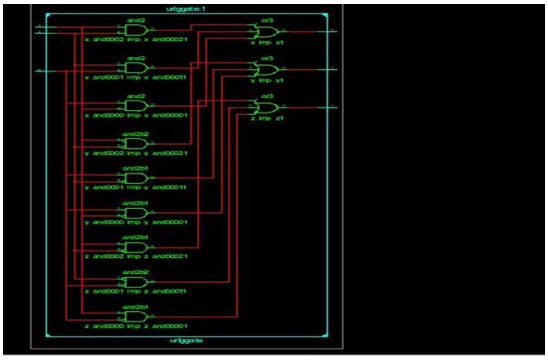

Fig. 4. RTL schematic of fredkin gate

B. RTL schematic of URL Gate

Here we designed the URLG. where A, B, C are inputs and X, Y, Z are outputs respectively. URLG consists of And gates, Or gates when can reduce gate count in complex circuits.

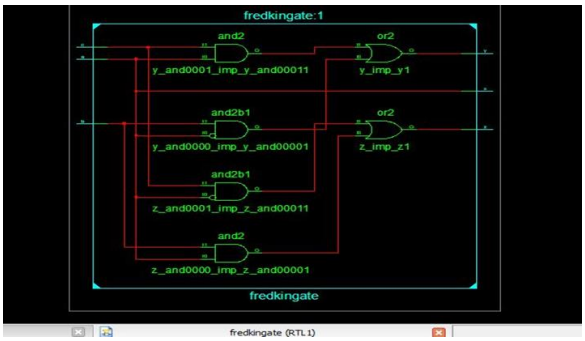

Fig. 5. RTL schematic of URL Gate

C. Simulation of Fredkin Gate

Here we simulated the Fredkin Gate and observed waveforms and they are met the our truth table specifications.

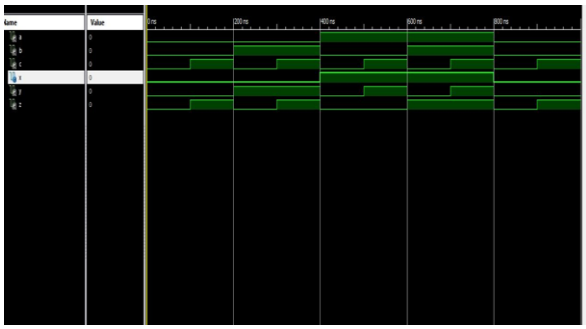

Fig. 6. Simulation of fredkin gate

D. Simulation of URLG

Here we simulated the URLG and observed the waveforms and they are met with our specifications of truth table.

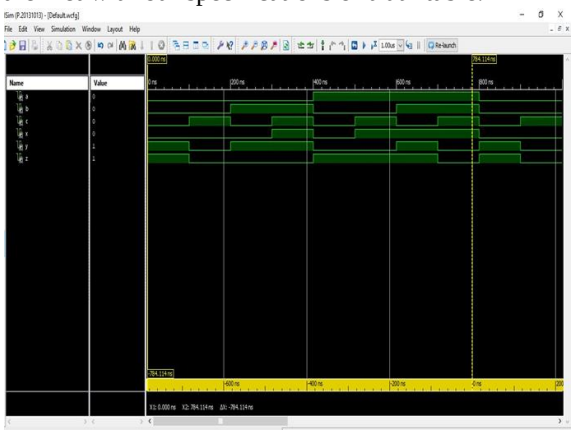

Fig. 7. Simulation of URLG

E. Design of priority encoder using reversible logic gates

Here we designed the priority Encoder which consists of Fredkin Gates and URLG.where I0, I1, I2 and I3 are four line inputs, Y1 and Y0 are the final encoded outputs which internally consists of xor, And gates and Or gates.

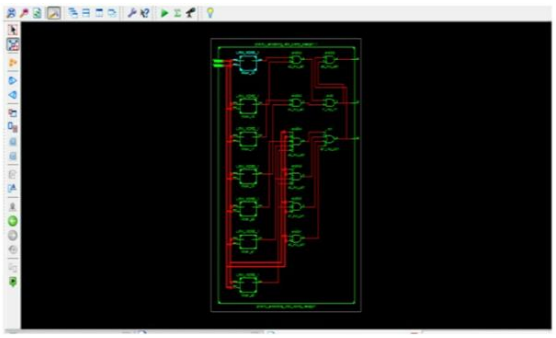

Fig. 8. Design of priority encoder using reversible logic gates

5. Conclusion

In this work, a reversible logic based design of 4x2 priority encoder is proposed and designed using Fredkin gate and URLG. The simulation results that the proposed design satisfies the truth table and the overall circuit performs only with two propagation delay.

6. Future scope

In this paper, we designed 4×2 priority Encoder Using Reversible Logic Gates. It can be further Enhanced to Low Power consumption higher order bits of priority Encoder and we can also design Low Power multipliers And control units And Alu's By using Reversible Logic Gates concept.

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